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Revision			
REV	DESCRIPTION	DATE	APPROVAL
1.0	INITIAL RELEASE		

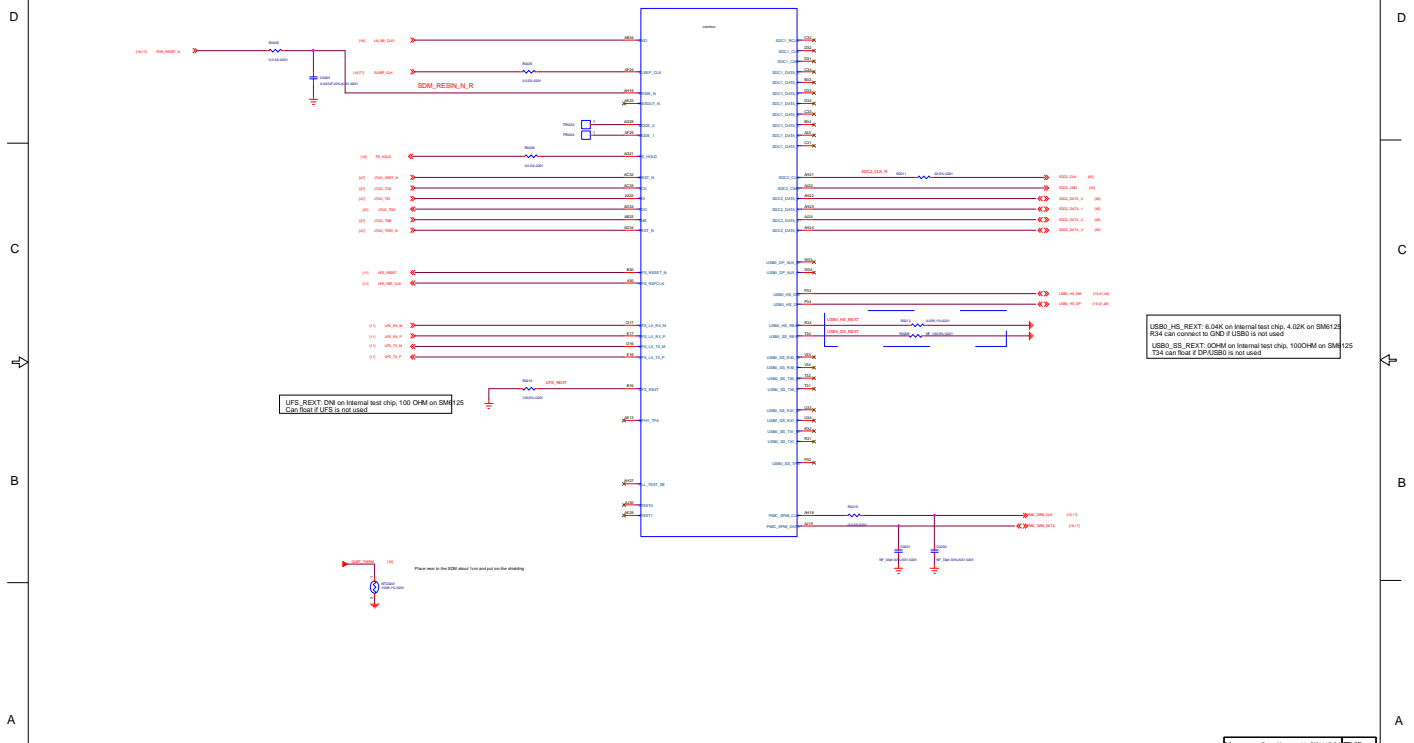
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UFS_REXT_DIN on Internal test chip, 100 Ohm on SM6125
 Can float if UFS is not used

USB0_SS_REXT_0 on Internal test chip, 4.02K on SM6125
 R34 can connect to GND if USB0 is not used
 USB0_SS_REXT_0OHM on Internal test chip, 100Ohm on SM6125
 R34 can float if DP/USB0 is not used

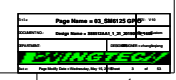
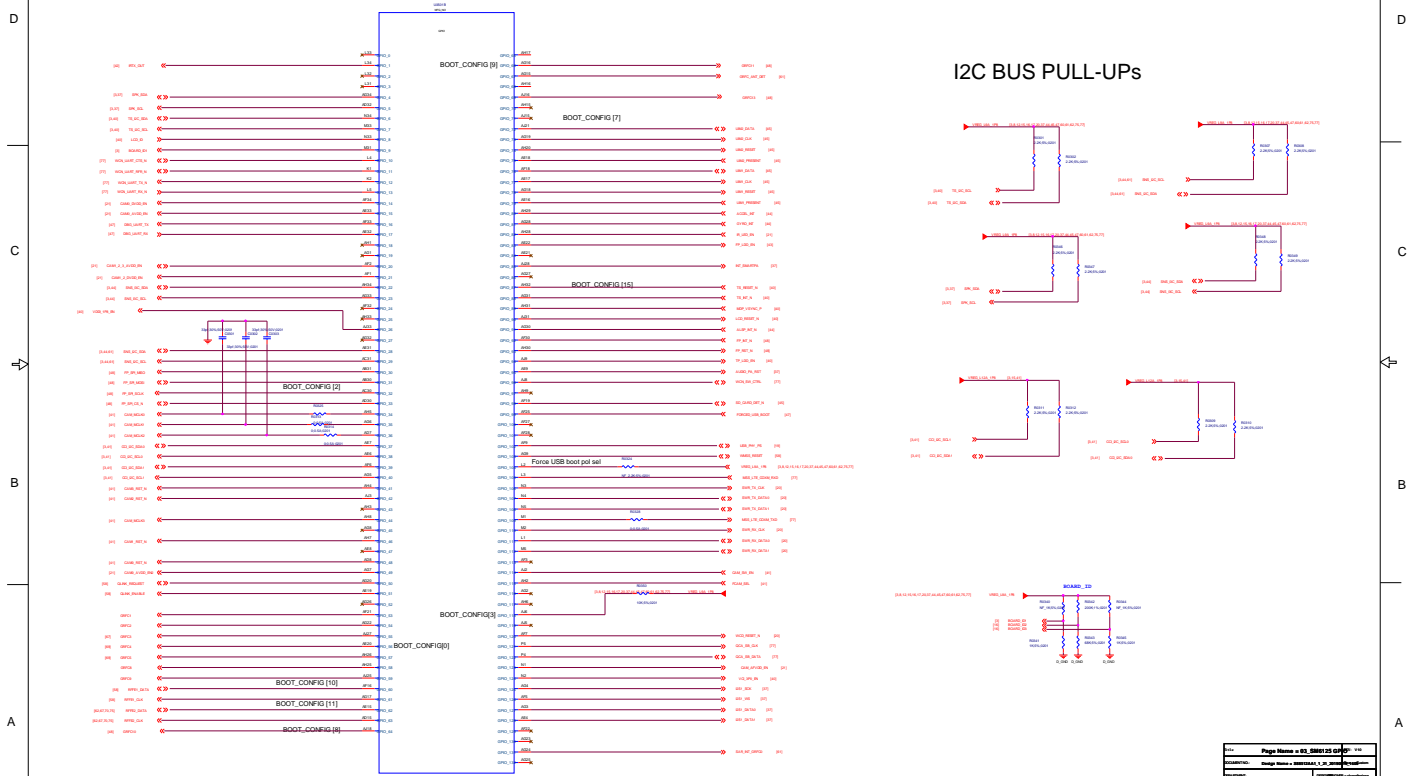
Please refer to the USB0 Pinout and pin list for wiring

SM6125 CONTROL



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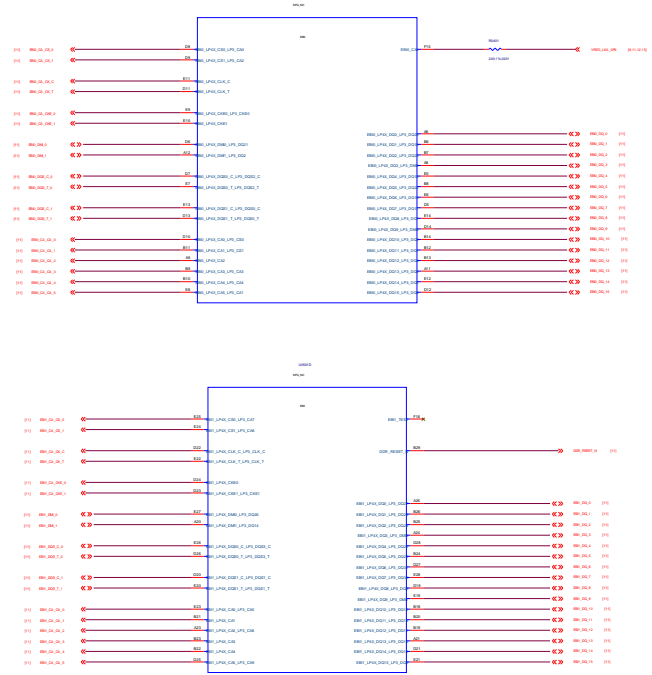
SM6125 GPIO

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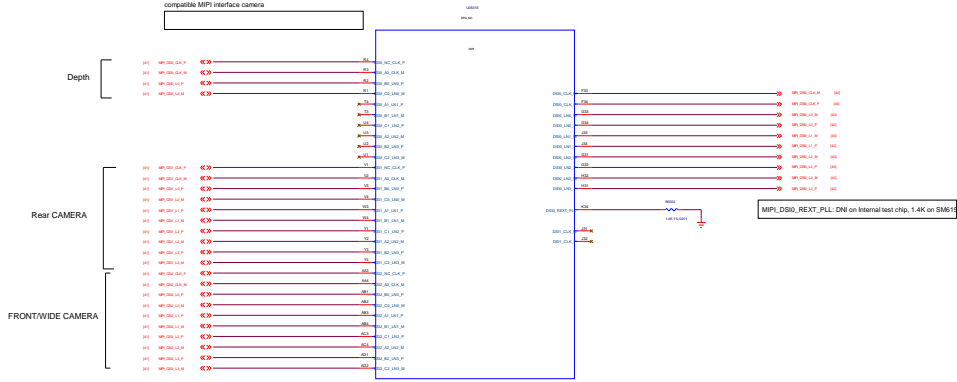


SM6125 EB10/1



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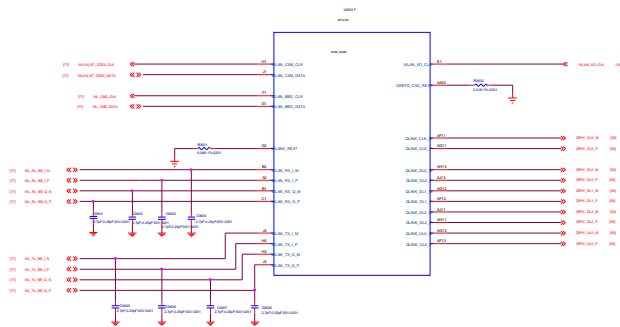


SM6125 MIPI-CSI/DSI



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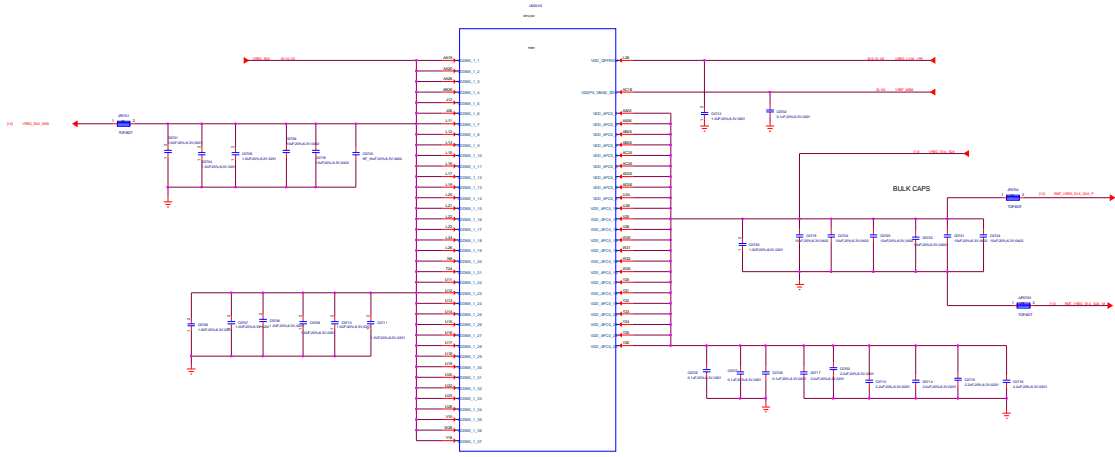
Add C1001-C1008 caps place holder for CLK decoupling to improve sensitivity.

SM6125 WCSS/RF



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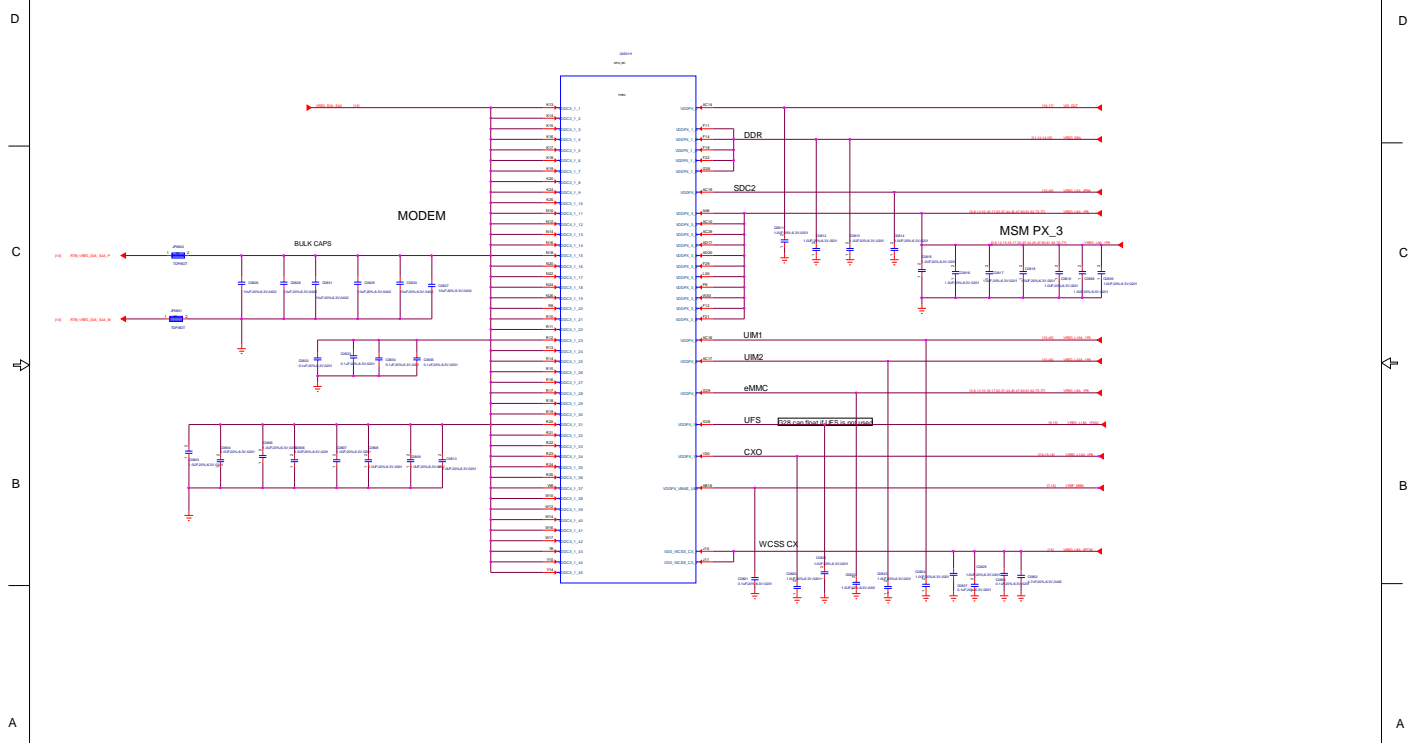


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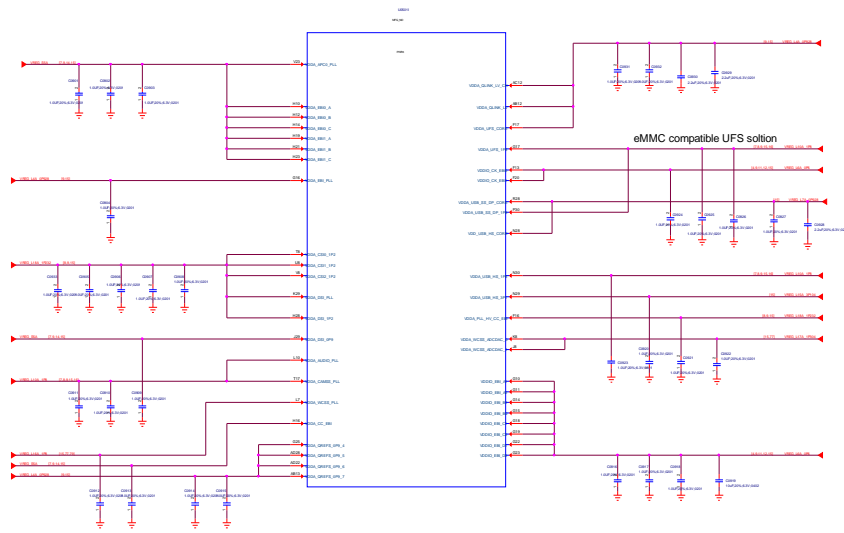


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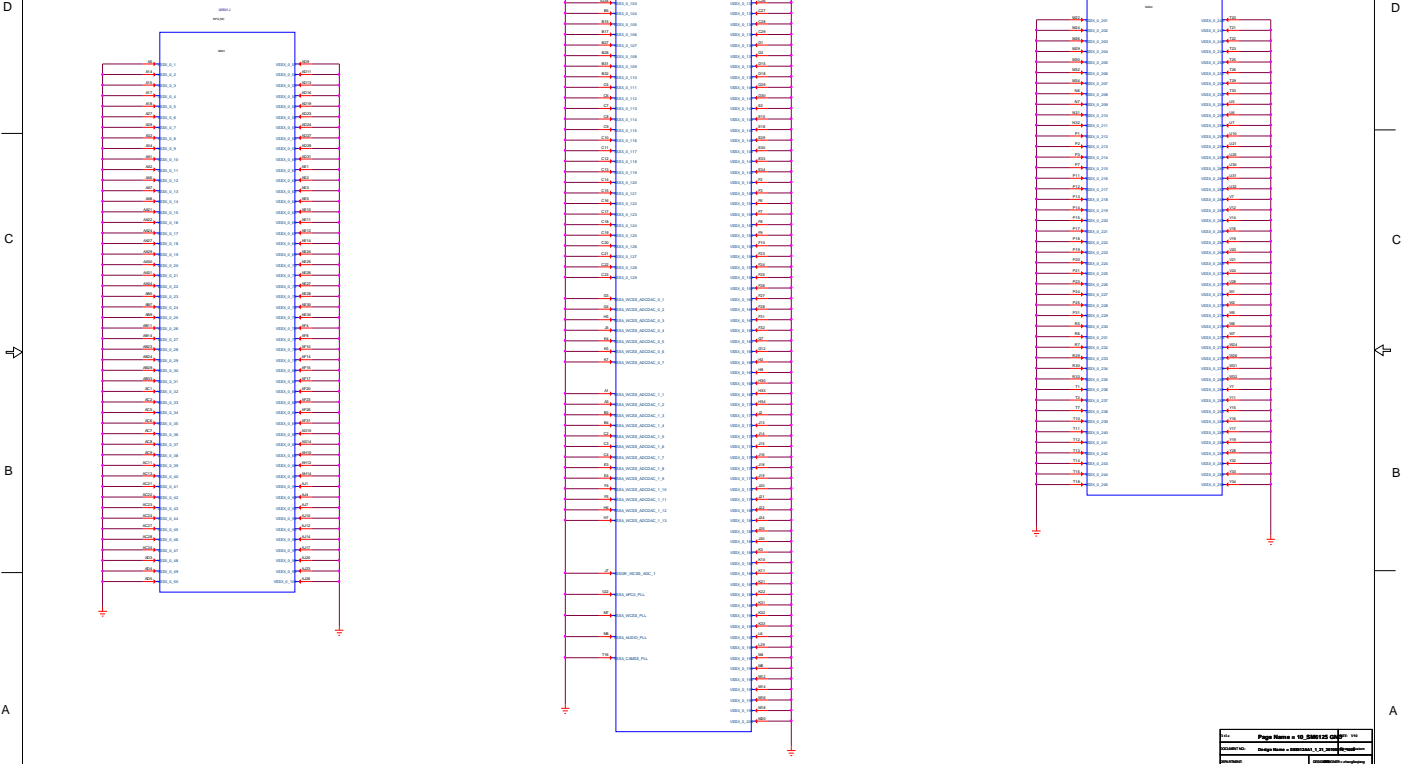


SM6125 PWR_3



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SM6125 GND

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Design Name = 10_208125_0001_000

DATE = 10/20/2007

TIME = 10:00:00

Author = [Redacted]

Checked = [Redacted]

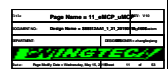
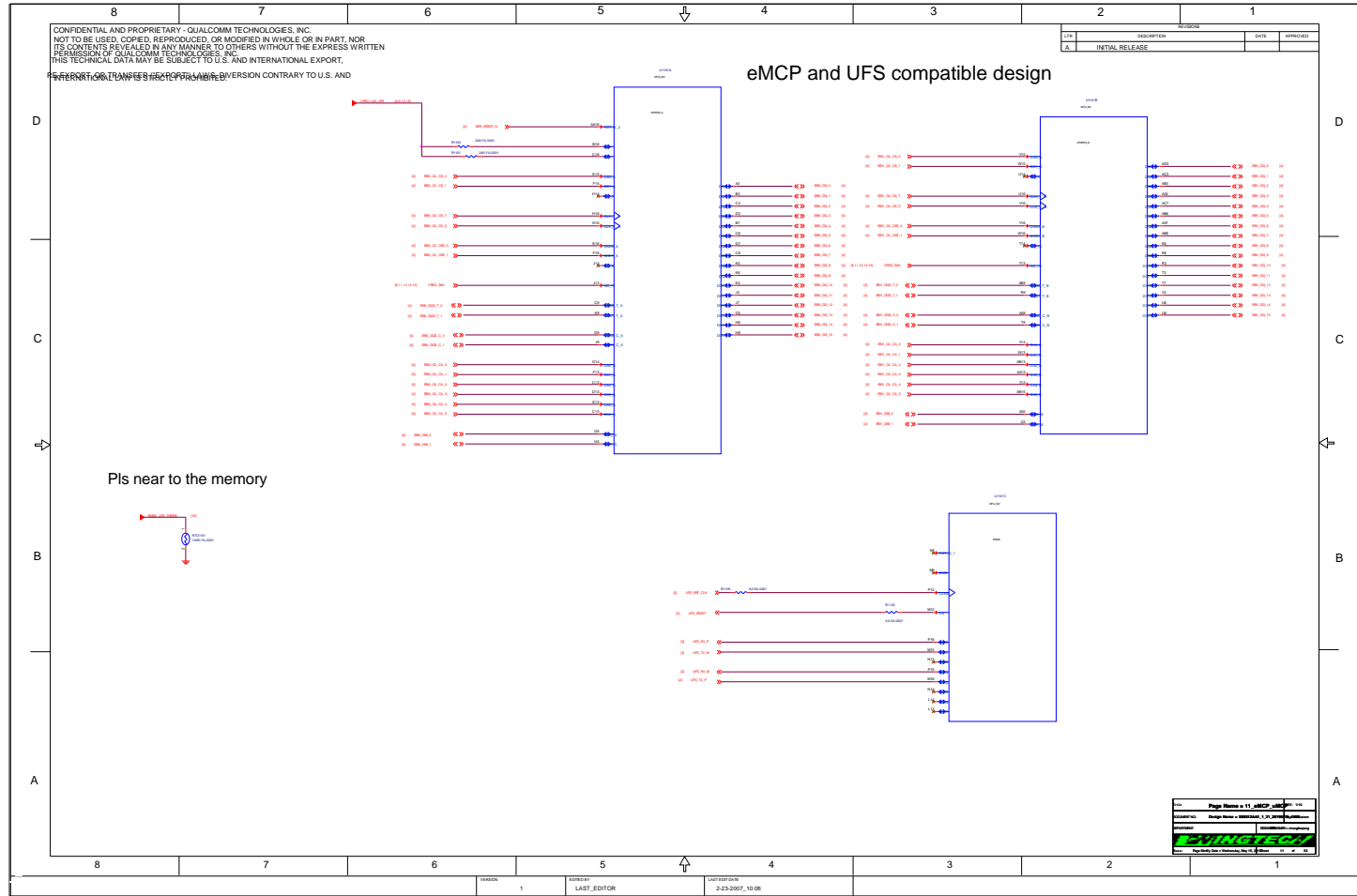
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PLATEWORK

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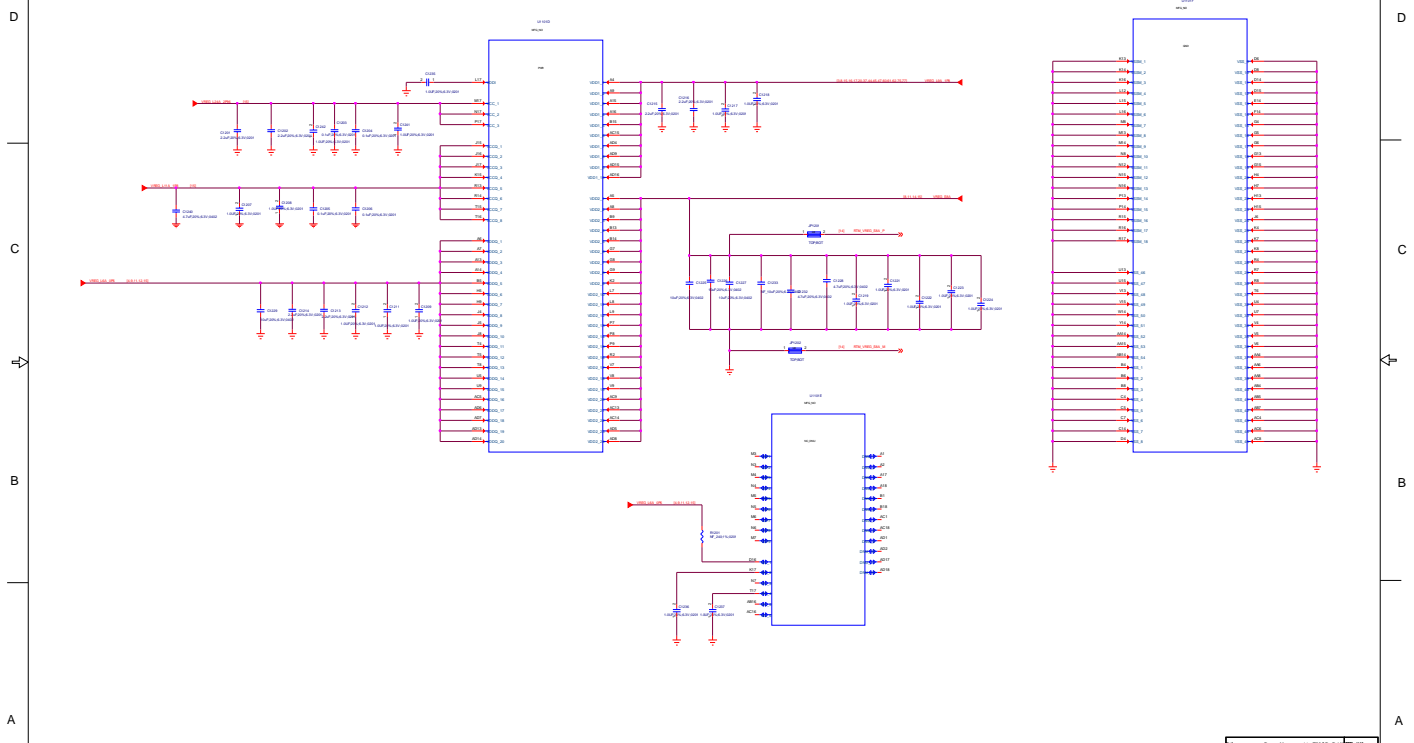
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emMCP and UFS compatible design



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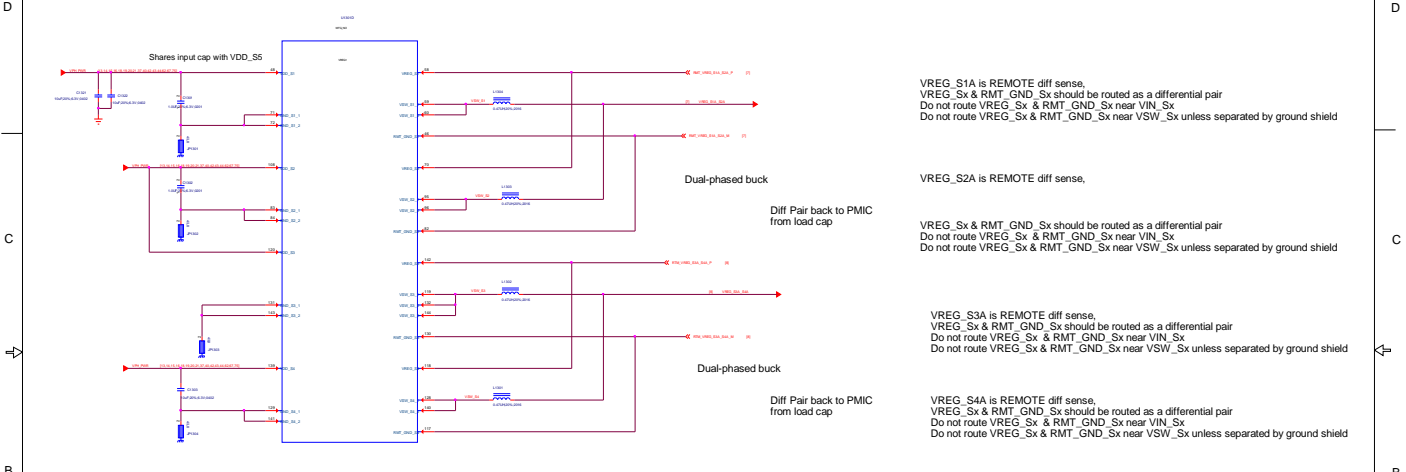
eMCP_POWER

Page Number: 12, eMCP_POWER_11
 Revision: 2-23-2007, 10:08
 Author: LAST_EDITOR
 Date: 2-23-2007, 10:08
 Drawing: eMCP_POWER_11.dwg
 Scale: 1:1
 Plot: 2/23/2007 10:08 AM

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VREG_S1A is REMOTE diff sense,
 VREG_Sx & RMT_GND_Sx should be routed as a differential pair
 Do not route VREG_Sx & RMT_GND_Sx near VIN_Sx
 Do not route VREG_Sx & RMT_GND_Sx near VSW_Sx unless separated by ground shield

VREG_S2A is REMOTE diff sense,
 VREG_Sx & RMT_GND_Sx should be routed as a differential pair
 Do not route VREG_Sx & RMT_GND_Sx near VIN_Sx
 Do not route VREG_Sx & RMT_GND_Sx near VSW_Sx unless separated by ground shield

VREG_S3A is REMOTE diff sense,
 VREG_Sx & RMT_GND_Sx should be routed as a differential pair
 Do not route VREG_Sx & RMT_GND_Sx near VIN_Sx
 Do not route VREG_Sx & RMT_GND_Sx near VSW_Sx unless separated by ground shield

VREG_S4A is REMOTE diff sense,
 VREG_Sx & RMT_GND_Sx should be routed as a differential pair
 Do not route VREG_Sx & RMT_GND_Sx near VIN_Sx
 Do not route VREG_Sx & RMT_GND_Sx near VSW_Sx unless separated by ground shield

Place Cin as close to PMIC as possible to achieve this requirement.
 Loop inductance from (VIN_Sx to Cin + Cin to GND_Sx) must be < 3nH

Nicobar Power Grid v1.31 10/31/2018

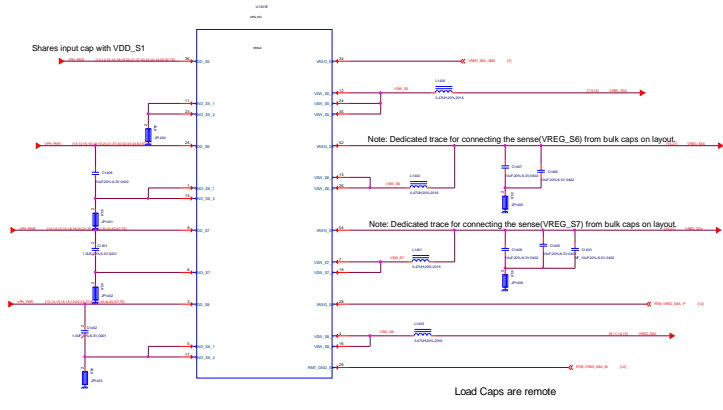
S1A-2A:	FTS510	0.8V default	8000mA lpeak	8110.00mA	APC
S3A-4A:	FTS510	0.8V default	8000mA lpeak	8480mA	CX, MODEM
S5A:	HFS510	0.912V default	4000mA lpeak	3620.00mA	EBI, MX, nLDO
S6A:	HFS510	1.352V default	4000mA lpeak	1560mA	LDO
S7A:	HFS510	2.04V default	2500mA lpeak	2350mA	LDO
S8A:	FTS510	1.128V default	4000mA lpeak	1790mA	LDO, LPDDR4x

PM6125_Bucks_S1-S4



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Place Cin as close to PMIC as possible to achieve this requirement.
 Loop inductance from (VIN_Sx to Cin + Cin to GND_Sx) must be < 3nH

Route diff pair out from Cap back to appropriate pins at PMIC

VREG_S8A is LOCAL diff sense,
 VREG_Sx & RMT_GND_Sx should be routed as a differential pair
 Do not route VREG_Sx & RMT_GND_Sx near VIN_Sx
 Do not route VREG_Sx & RMT_GND_Sx near VSW_Sx unless separated by ground shield

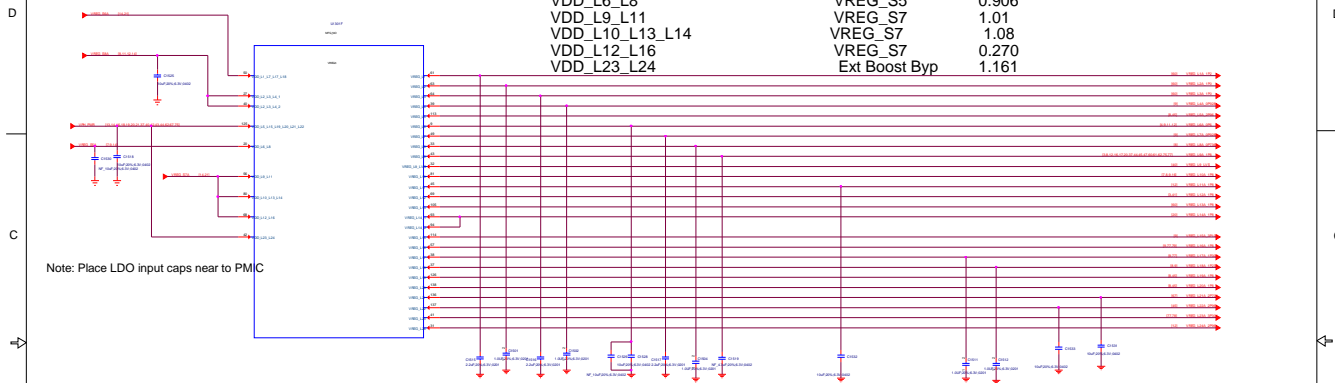
PM6125_Bucks_S5-S8

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LDO Input Rail	Parent Buck	Max Current
VDD_L1_L7_L17_L18	VREG_S6	1.13
VDD_L2_L3_L4	VREG_S8	0.816
VDD_L5_L15_L19_L20_L21_L22	Ext Boost Byp	1.38
VDD_L6_L8	VREG_S5	0.906
VDD_L9_L11	VREG_S7	1.01
VDD_L10_L13_L14	VREG_S7	1.08
VDD_L12_L16	VREG_S7	0.270
VDD_L23_L24	Ext Boost Byp	1.161

DESCRIPTION	DATE	APPROVED
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Nicobar Power Grid v1.31 11/12/2018

LDO Type Source V_default (est) Target Pin#

L1 N600	S8A 1.2V (625) QLN SDR 1.2 61
L2 N300	S8A 1V (320) SDR VDD 1.0V 63
L3 N600	S8A 1V (370) SDR VDD 1.0V 64
L4 N300	S8A 0.925V (129) QLINK, EBI, MIPI 39
L5 MVP50	VPH 2.96V (22) PX 113
L6 N1200	S8A 0.624V (1040) VDDQ, EBI 9
L7 N600	S8A 0.925V (64-2) USB 49
L8 N300	S8A 0.864V (81) CX 33
L9 LVP600	STA 1.8V (754) Sensors, WCD, TMD, PMI, MSM, QET 43
L10 LVP150	STA 1.8V (100) QFPROM, USB,UFS, PX 81
L11 LVP600	STA 1.8V (925) EMMC/VCCQ 45
L12 LVP300	STA 1.8V (121) DV, USB, REDRIVER 69
L13 LVP300	STA 1.8V (204) QPM 1.8V, BBRX, GPS 105
L14 LVP600	STA 1.8V (650) WCD Buck 94.93
L15 MVP150	VPH 3.125V (5.25) USB 3.1V, DP, PHY 114
L16 LVP150	STA 1.8V (92.5) WCSS, WCN, XO 93
L17 N300	S8A 1.304V (246) WCN, WCSS ADX DAC 38
L18 N300	S8A 1.235V (133) MIPI, VDDPX 37
L19 MVP150	VPH/BB 1.8V (60.2) Memory, SN100, PX 126
L20 MVP150	VPH/BB 1.8V (60.2) Memory, SN100, PX 138
L21 MVP600	VPH/BB 2.704V (0.68) CAT, DFE, RTC, QSW 136
L22 MVP600	VPH/BB 2.96V (600) MMC 137
L23 MVP600	VPH/BB 3.304V (591) WCN 3.3V 41
L24 MVP600	VPH/BB 2.96V (1170) EMMC 31

LDO L5/L9/L10/L11/L12/L13/L14/L15/L16/L19/L20/L21/L22/L23/L24 is the Pseudo-capless LDO, so can dnt CAP in BOM
 PSEUDO CAPLESS LDOs
 P-type are pseudo-capless, cap can be at load
 For CAPLESS LDOs: If decaps on the load side do not
 add up to LDO spec, then install the cap close to the PMC

1.0uF

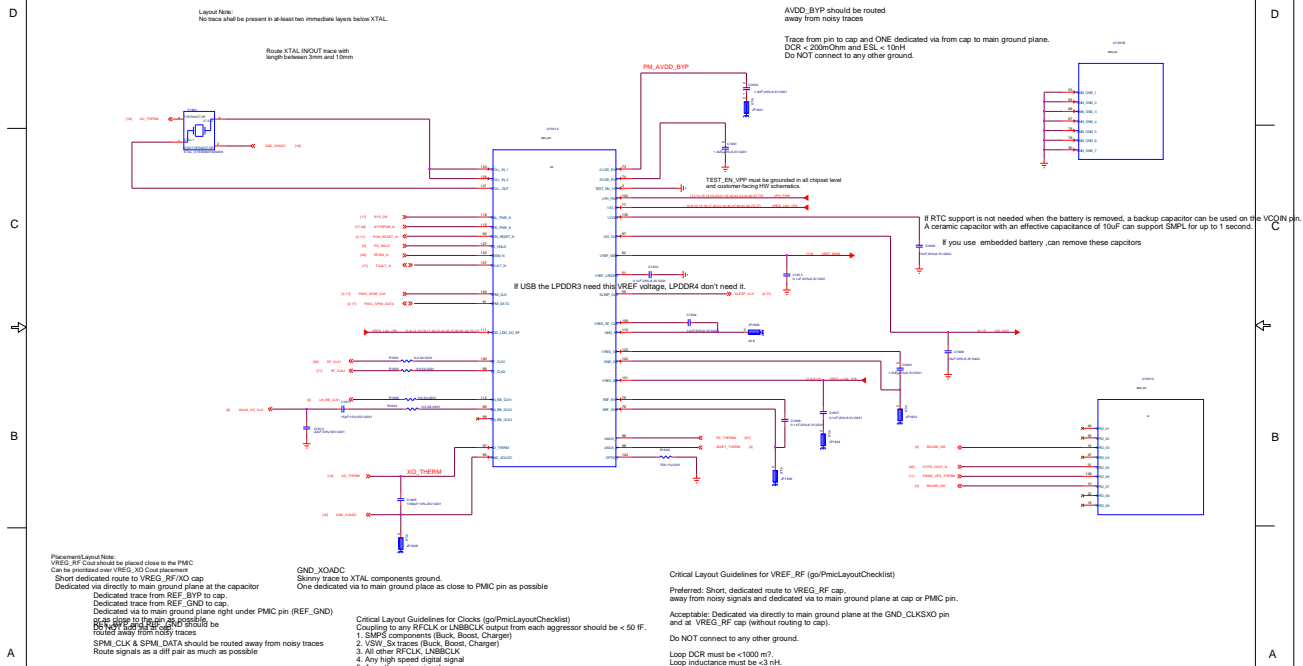
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PM6125_LDOs



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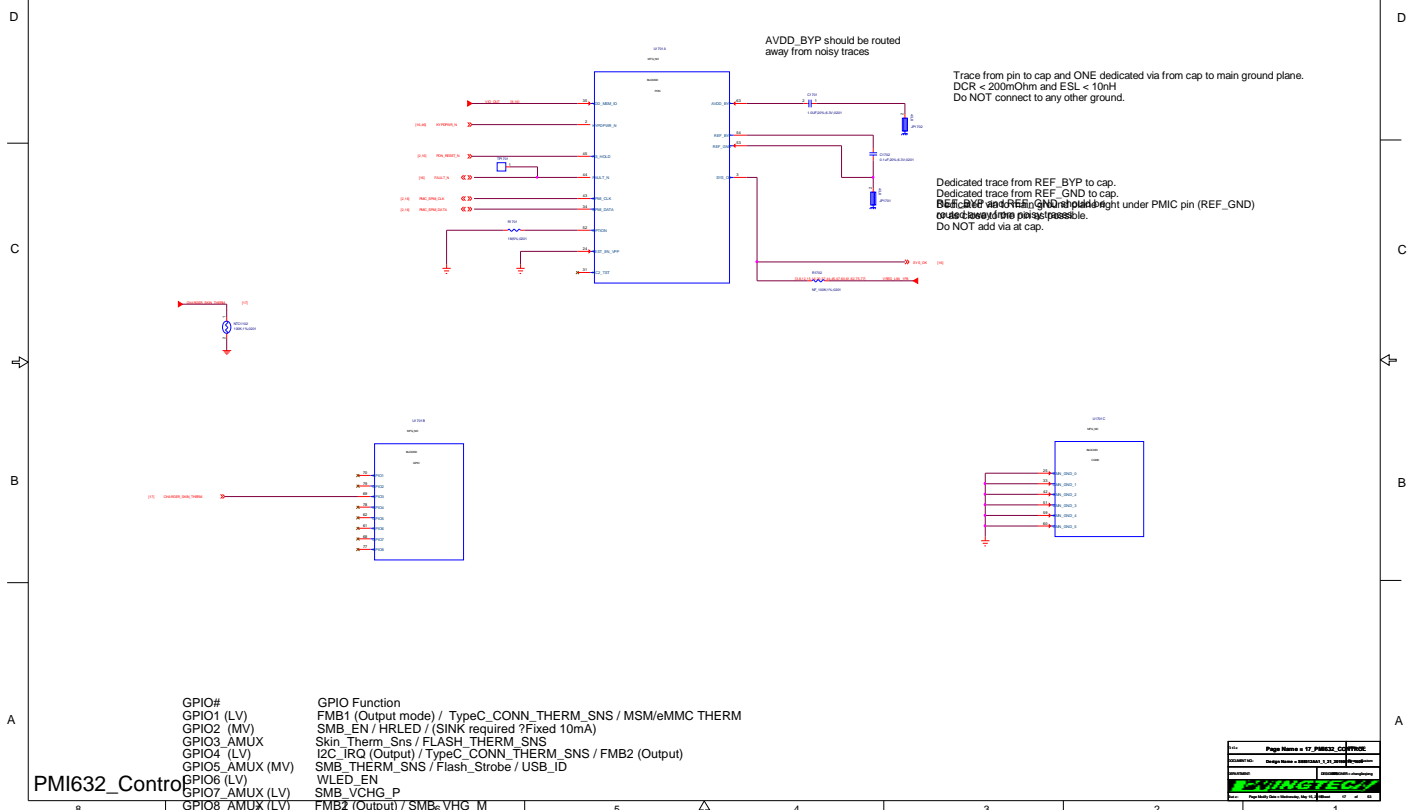


PM6125_HK/IO



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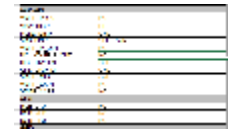
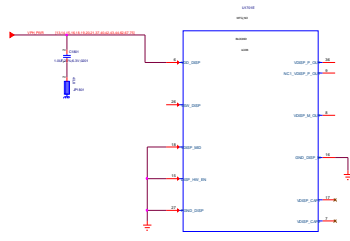
PM1632_Contro

GPIO#	GPIO Function
GPIO1 (LV)	FMB1 (Output mode) / TypeC_CONN_THERM_SNS / MSM/eMMC THERM
GPIO2 (MV)	SMB_EN / HRLD / (SINK required ?Fixed 10mA)
GPIO3_AMUX	Skin_Therm_Sns / FLASH_THERM_SNS
GPIO4 (LV)	I2C_IRQ (Output) / TypeC_CONN_THERM_SNS / FMB2 (Output)
GPIO5_AMUX (MV)	SMB_THERM_SNS / Flash_Strobe / USB_ID
GPIO6 (LV)	WLED_EN
GPIO7_AMUX (LV)	SMB_VCHG_P
GPIO8_AMUX (LV)	FMB2 (Output) / SMB_VHG_M

Rev	Page Name = 17_PMI632_Controller
Author	Design Name = PM1632_Contro
Checker	Location = Qualcomm
Approved	Part Number = PM1632_Contro

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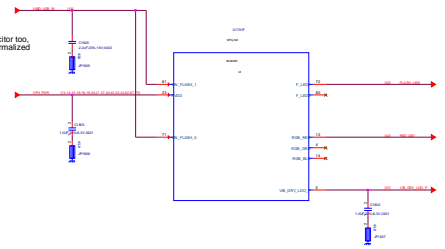
DATE	DESCRIPTION	DATE	APPROVED
01	INITIAL RELEASE		



Layout Note: VDISP_CAPx
Place fly cap as close to the pin as possible.
Avoid routing VDISP_CAP1 trace under VDISP_M_OUT.

Layout Note: DISP_HW_EN
This signal is used for "Display Tap to Wake"
If unused in HW, this pin should be connected to GND

NOTE:
C2404 can use the 25V capacitor too,
just for the BOM category normalized



PMI632_LCD/IB/RGB/Flash



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NOTE:
Use C1902= 2.2uF for parallel Charging Config
Use C1902= 4.7uF for only Fast Charging Config

NOTE:
C1902 can use the 25V capacitor too,
just for the BOM category normal

Layout Note:
PACK_SNS_M should have a dedicated route
Necessary connector negative sense
recommend to use battery NTC values 100K, B=4250

CAD NOTE:
Dedicated VIA to Main GND

NOTE:
BOOT_PWR net is 5VDC.cap is 0603. Do not use 0402 as may derate to ~80%.

CAD NOTE:
Dedicated VIA to Main GND

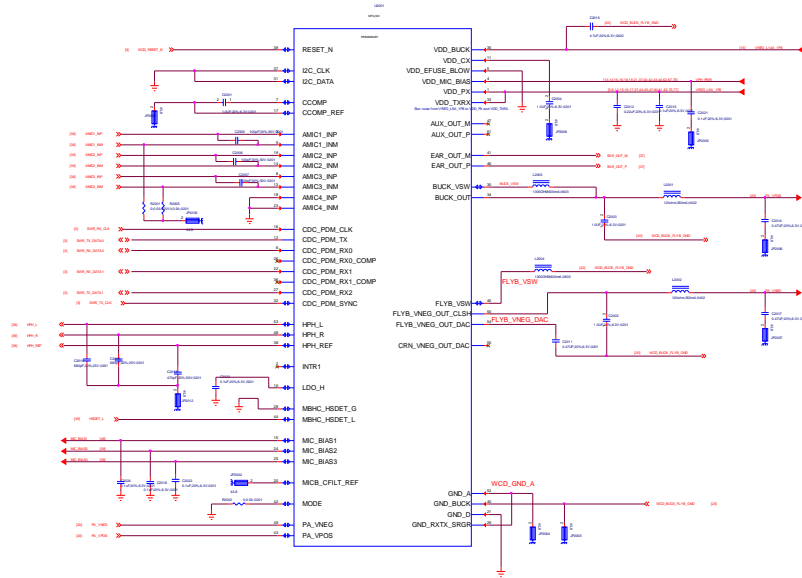
REV	DESCRIPTION	DATE	APPROVED
1.0	METAL RELEASE		

PMI632_Charger/PD PHY



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TRX	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE		



WCD9370

REV	Page Name + ID	REV	DATE
1	WCD9370	1	2-23-2007 10:06

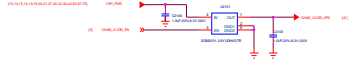
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REVISION			
DATE	DESCRIPTION	DATE	APPROVAL
2.0	INITIAL RELEASE		

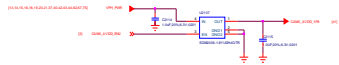
800mA LDO for Rear Camera (CAM0_DVDD_1P1)



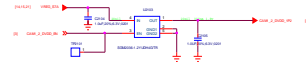
LDO for Rear Camera (VCAMA_EXT) 2.9V



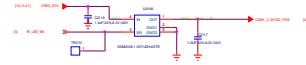
LDO for Rear Camera (VCAMA_EXT) 1.8V



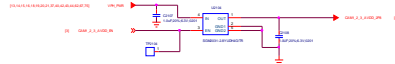
LDO for CAM1_2_DVDD_1P2



LDO for CAM1_2_DVDD_1P05



LDO for CAM1_2_3_AVDD_2P8



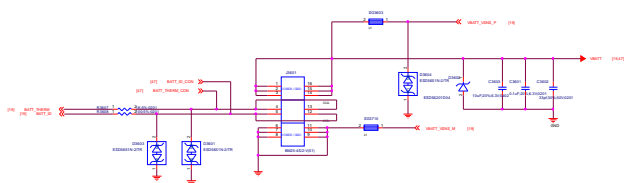
LDO for CAM_AF_2P8兼容TP2.8V



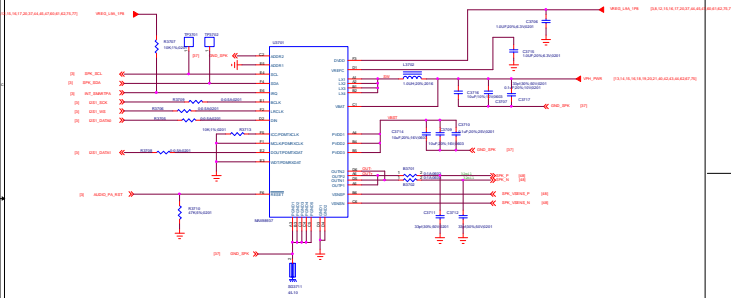
CAM eLDOS

Page Name	Page No.
21_CAM eLDO	10
Author	Wang, Xiang
Reviewer	Wang, Xiang
Approvers	
Page Size	10.00 x 10.00

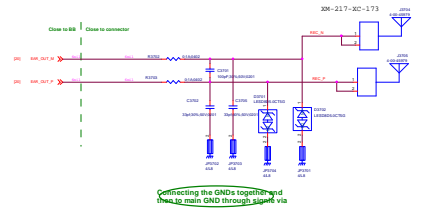
BATTERY CONNECTOR



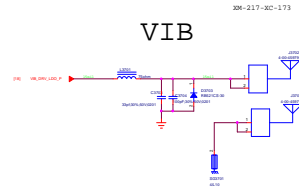
SPK



Receiver

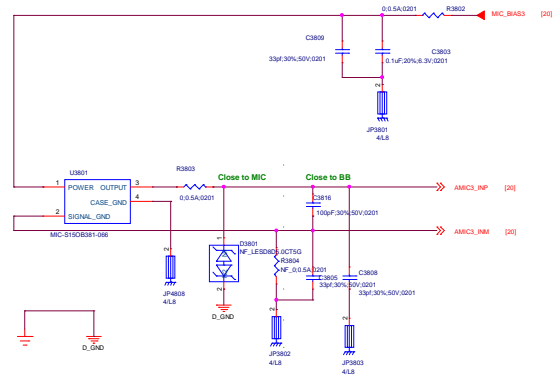
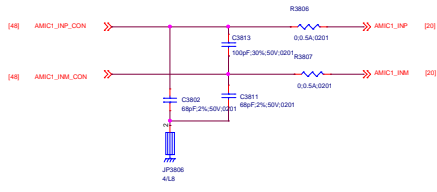


VIB



Handset 2nd Microphone (Rear - DMNR), AMIC

MAIN MIC

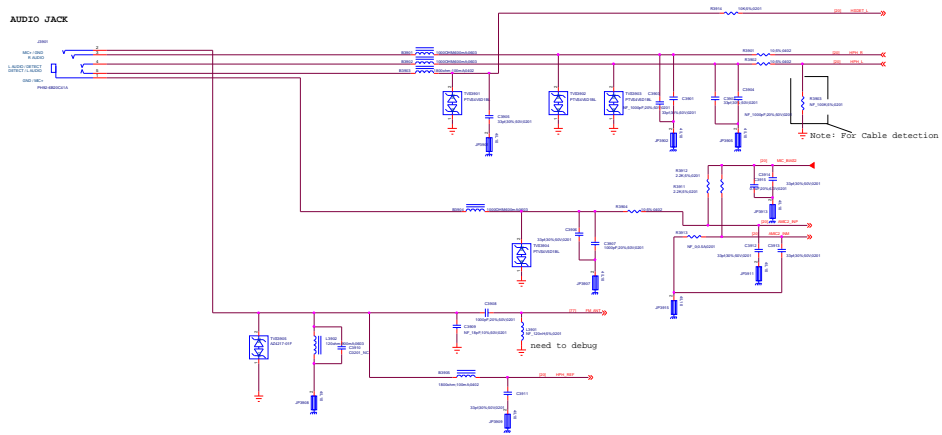


Schematic design notice of "63_PERI_AUDIO_IO" page.

Note 63-1: 1 uF for ACC mode

Page Name = 30_MIC	REV: V10
DOCUMENT NO: Design Name = S88512AA1_1_21_201905	DESIGNER: C
DEPARTMENT: DESIGN/ENGINEER = shengjiejing	
EVINGTECH	
Date: Page Modify Date = Wednesday, May 15, 2019	38 of 53

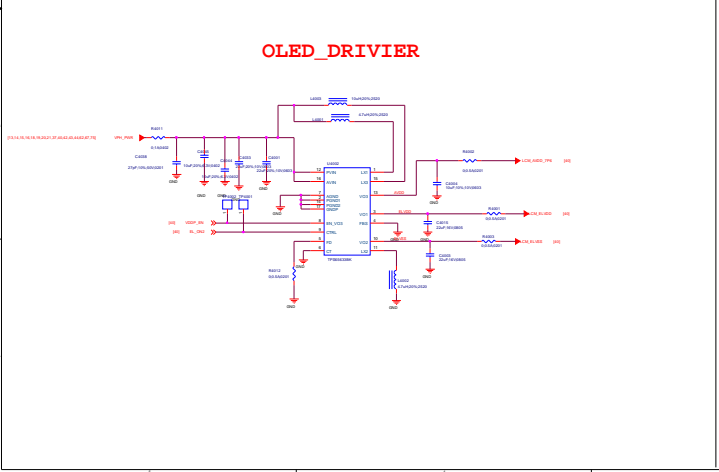
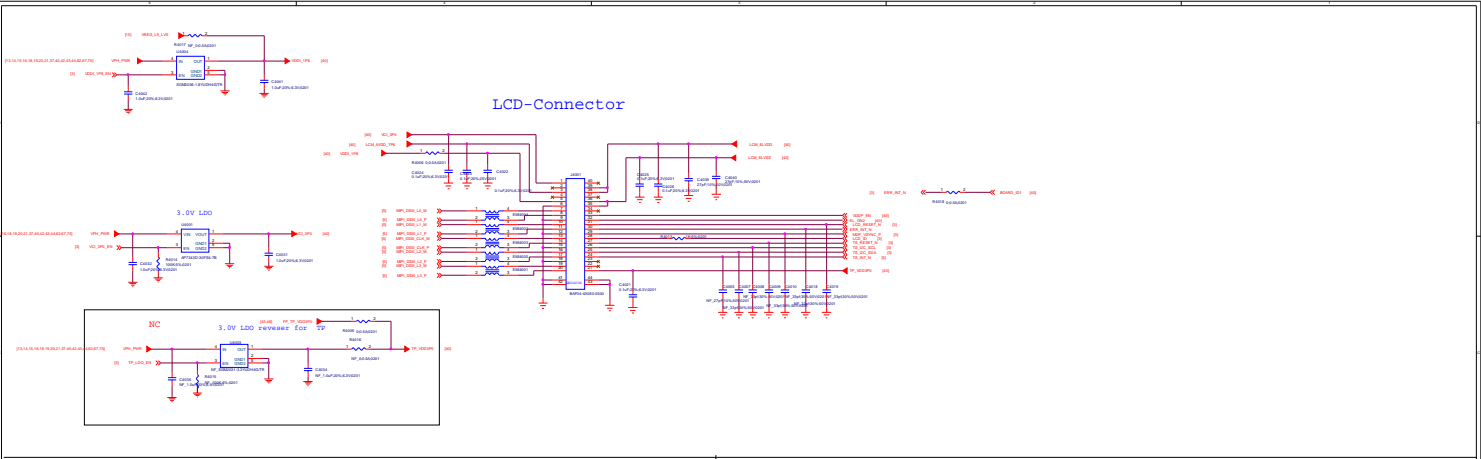
AUDIO JACK



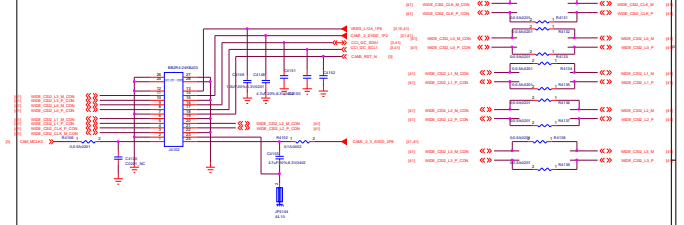
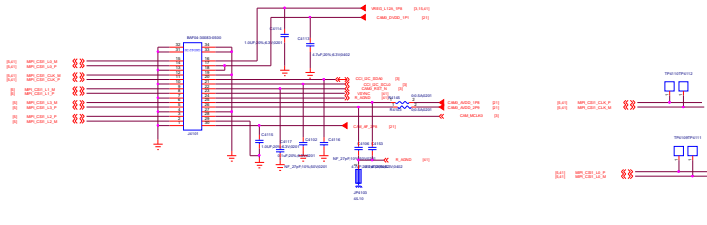
Note: Ferrite beads and their corresponding bypass capacitors on CDC_RPR_L_P, CDC_RPR_L_M and CDC_RPR_RPF are needed to reduce noise generated by audio/FM concurrency

Note: F02 Cable detection

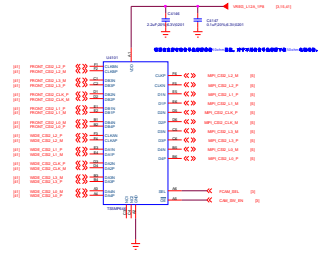
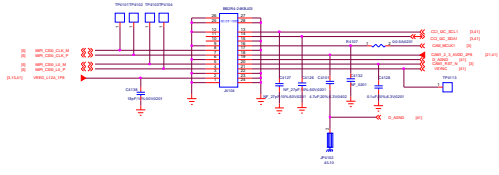
need to debug



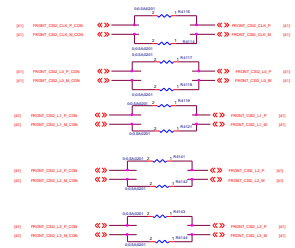
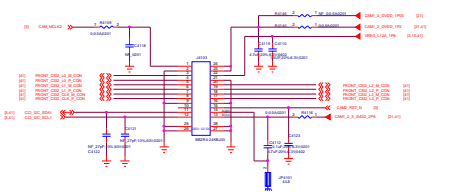
Main Camera



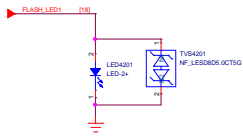
Depth Camera



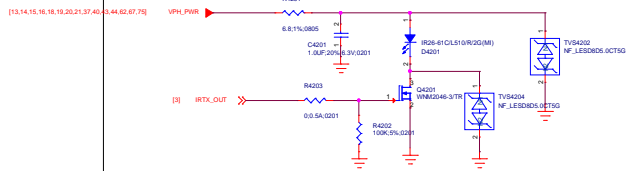
Front Camera



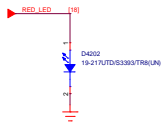
FLASH_DRIVER



IR_LED

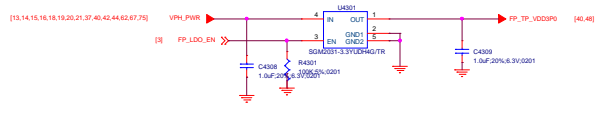


LED_DRIVER



File:	Page Name = 42_Flash/RGB	REV: V10
DOCUMENT NO.:	Design Name = 88812AA1_1_21_201908	REV: C
DEPARTMENT:	DESIGNER/ENGINEER = zhangyongqiang	
WINGTECH		
Net:	Page Modify Date = Wednesday, May 13 2014	42 of 53

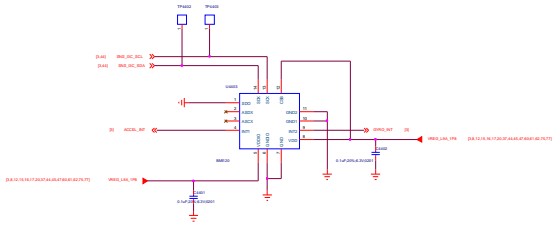
FP LDO 3.0V



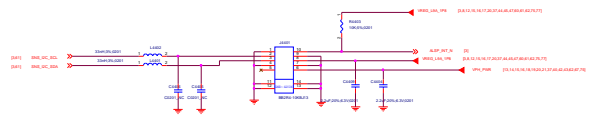
Page Name = 43_Fingerprint	REV: V10
DOCUMENT NO.: Design Name = 88813A01_1_21_201905	DESIGNER: C
DEPARTMENT:	DESIGNER/EAER = shung-shung
WINGTECH	
File: Page Modify Date = Wednesday, May 13, 2020	43 of 55

ACCELEROMETER

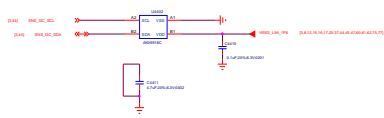
A+G SENSOR

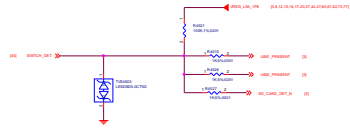
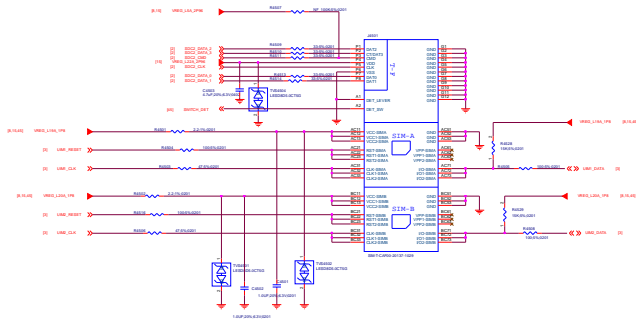


ALP-SENSOR

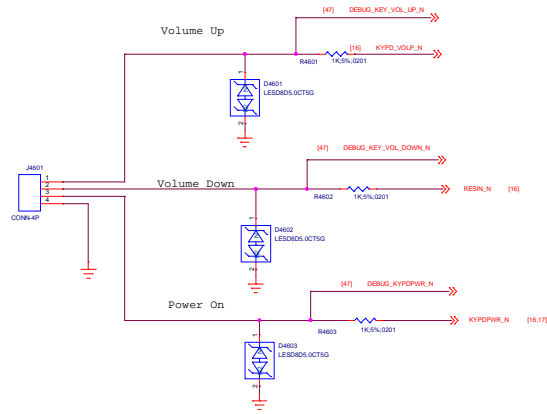


Magnetic Sensor





Keys



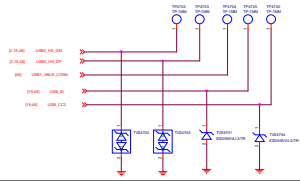
Schematic design notice of "75_PERI_KEYPAD" page.

Note 75-1: DO NOT put pull-up resistor on PWRKEY

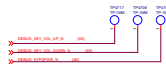
Note 75-2: Volume Up : HOME Key / GND
Volume Down : KPROW0/KPCOL0

Page Name = 46_Sidekey	REV: V10
DOCUMENT NO.: Design Name = 026012AA1_1_31_201908	DESIGNER: C
DEPARTMENT:	DESIGNER: shangshang
WINTECH	
Page Modify Date = Wednesday, May 13 2020 48 of 53	

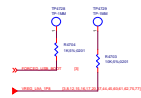
USB



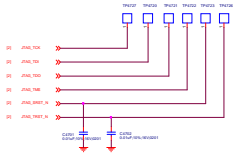
KEYS



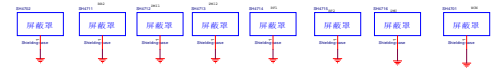
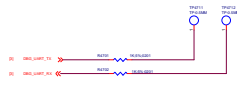
TEST



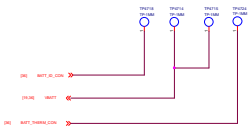
JTAG CONNECTOR



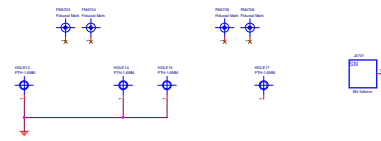
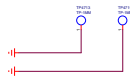
UART



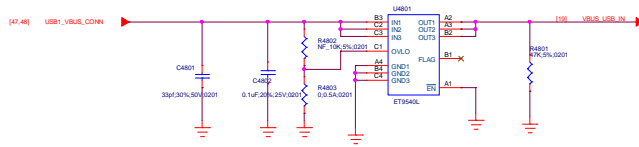
BATTERY



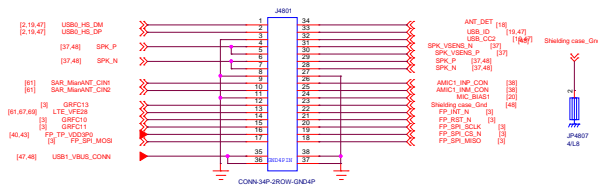
GND




OVP



Sub Board Connector



		SECTION							
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A.1		INITIAL RELEASE							
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		1		LAST_EDITOR		3-23-2007 10:06			

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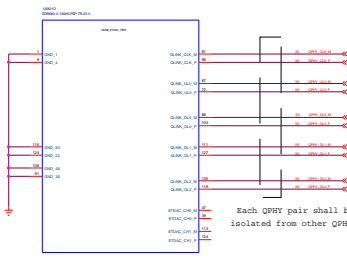
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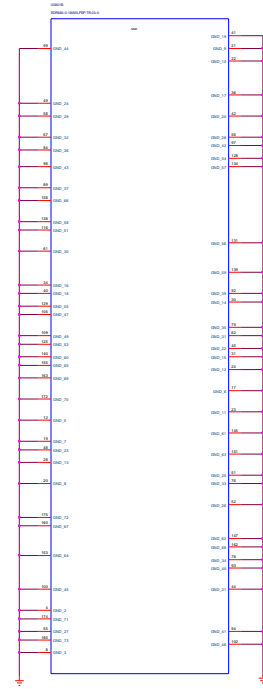
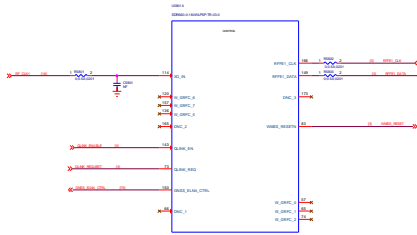
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SDR660 MSS & GND

REVISIONS			
TRX	DESCRIPTION	DATE	APPROVED
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NOTE:
 One dedicated RFFE bus is required for SDR660 debug purposes



SDR660_MSS_GND

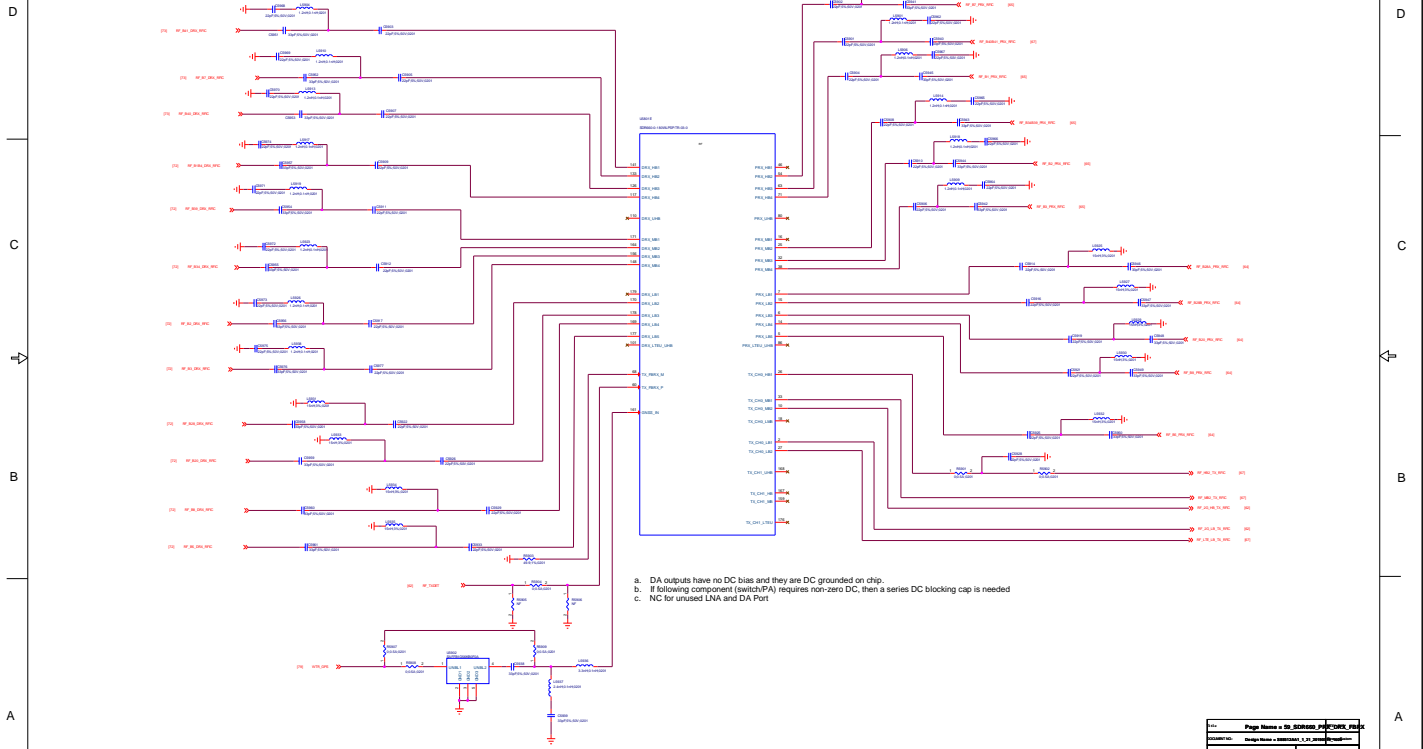
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Revisions			
LTN	Description	Date	Approved
1	INITIAL RELEASE		

SDR660 Tx, PRX, DRX, FBRX



- a. DA outputs have no DC bias and they are DC grounded on chip.
- b. If following component (patch/PA) requires non-zero DC, then a series DC blocking cap is needed
- c. NC for unused LNA and DA Port

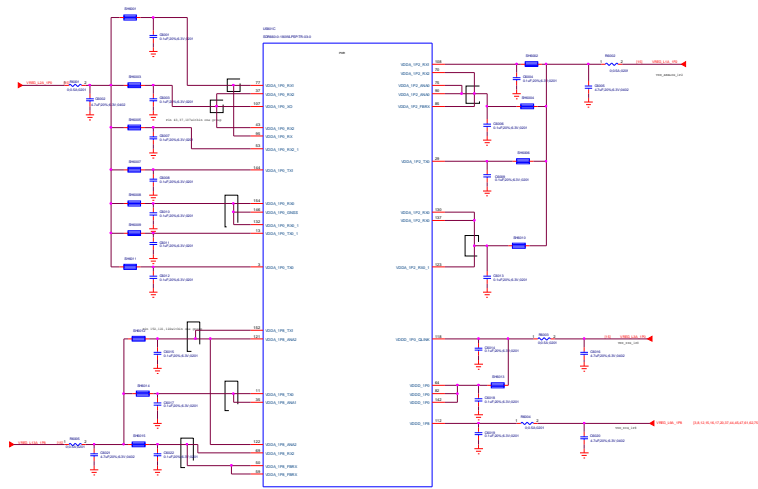
SDR660_PRX_DRX_FBRX



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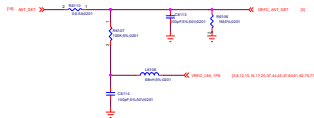
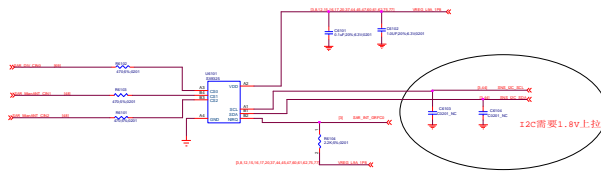
REVISION			
TR	DESCRIPTION	DATE	APPROVED
1	INITIAL RELEASE		

SDR660 POWER



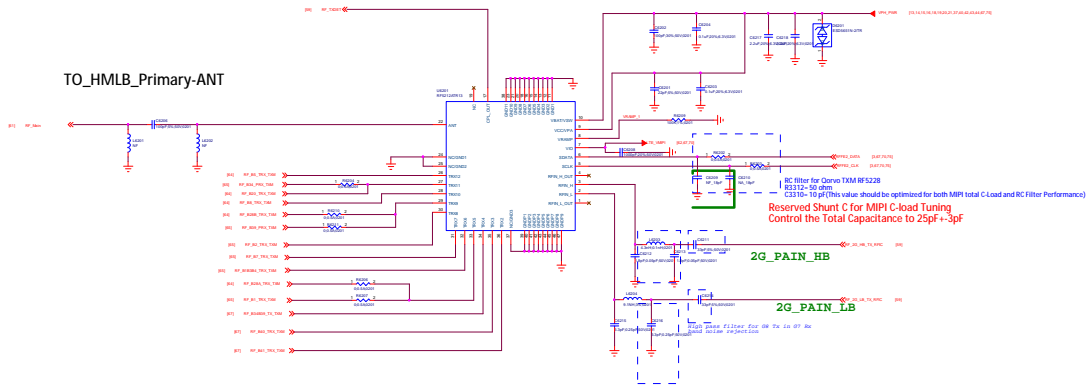
SDR660_PWR





DATA IN/OUT FROM HMLB PRIMARY PARTS

TO_HMLB_Primary-ANT

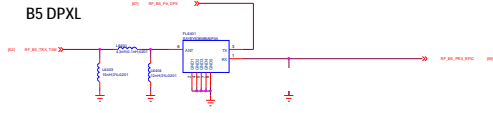


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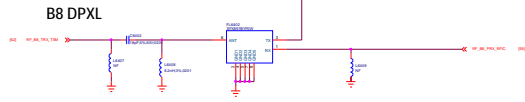
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REV	DESCRIPTION	DATE	APPROVED						
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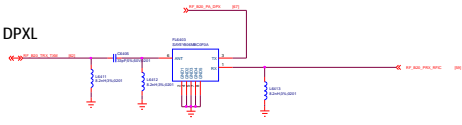
B5 DPXL



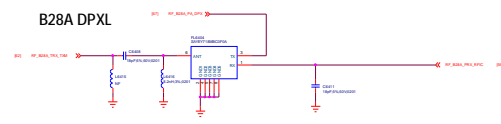
B8 DPXL



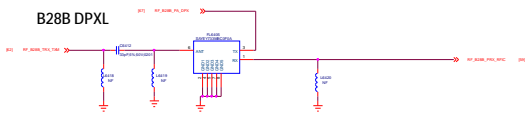
B20 DPXL



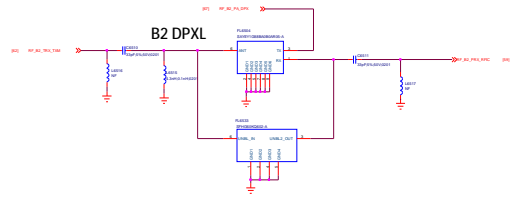
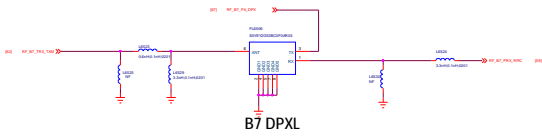
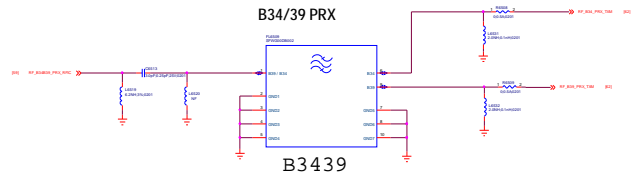
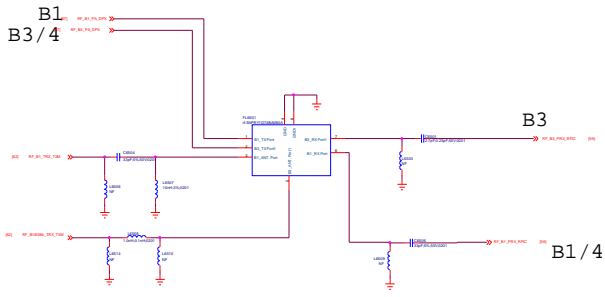
B28A DPXL

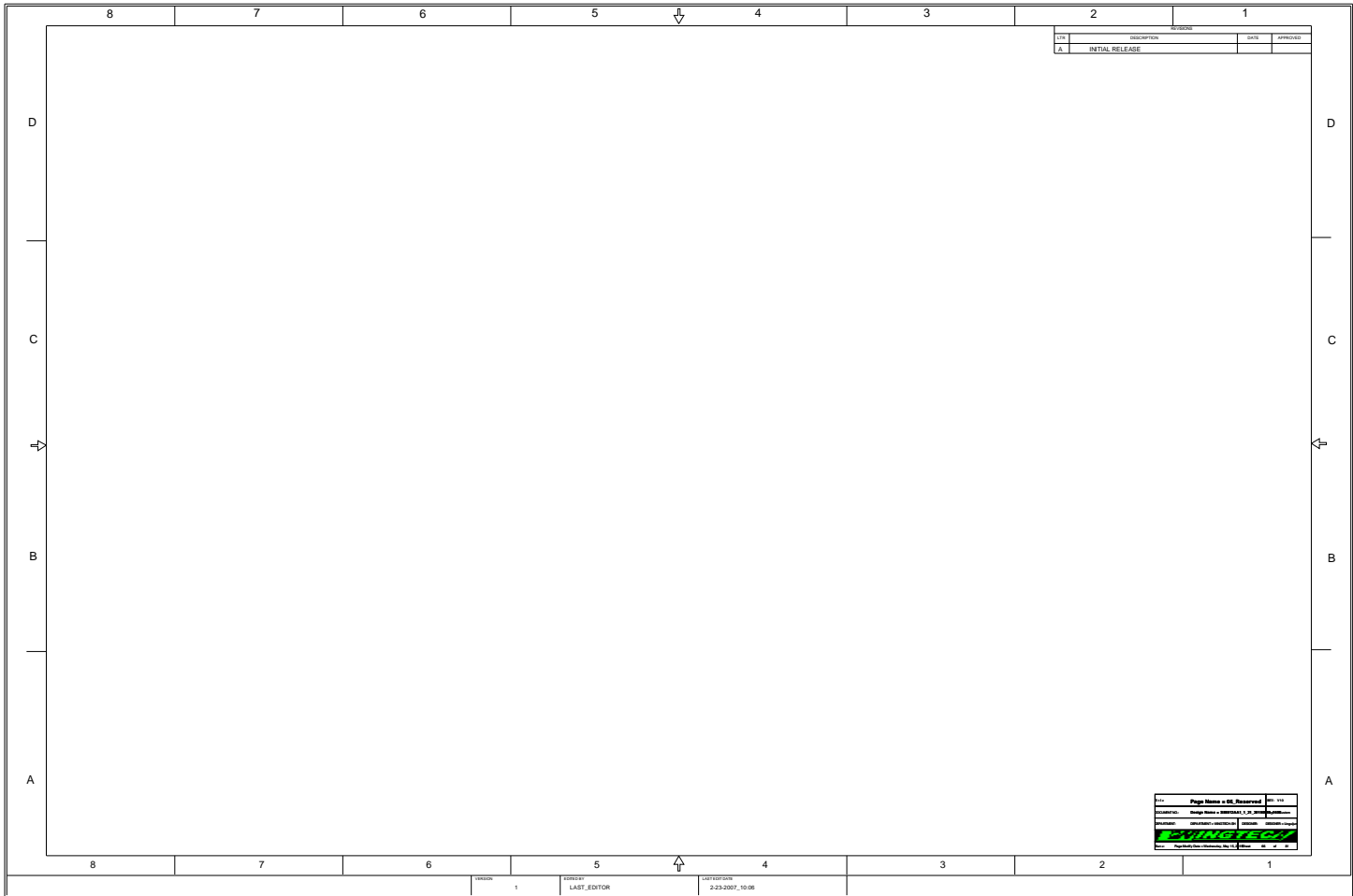


B28B DPXL



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海外版使用四工器，两者做兼容。





REV	DESCRIPTION	DATE	APPROVED
1	INITIAL RELEASE		

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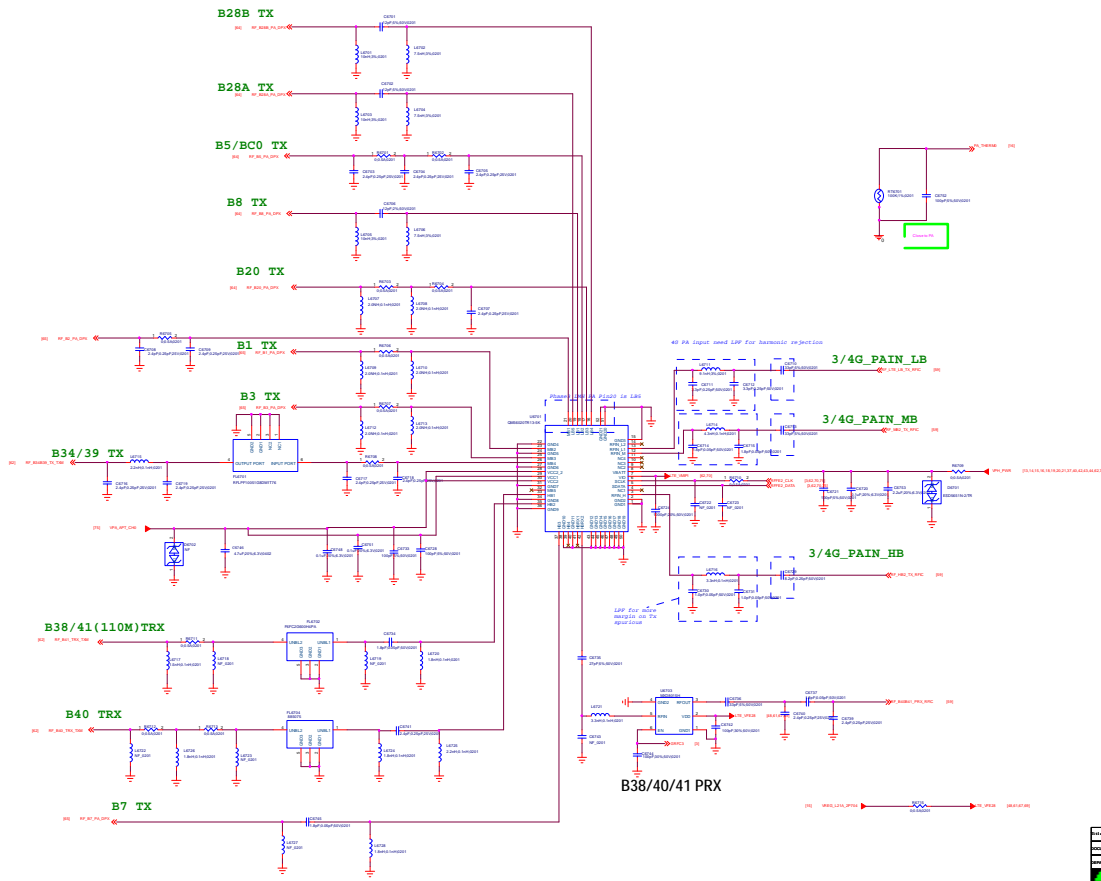
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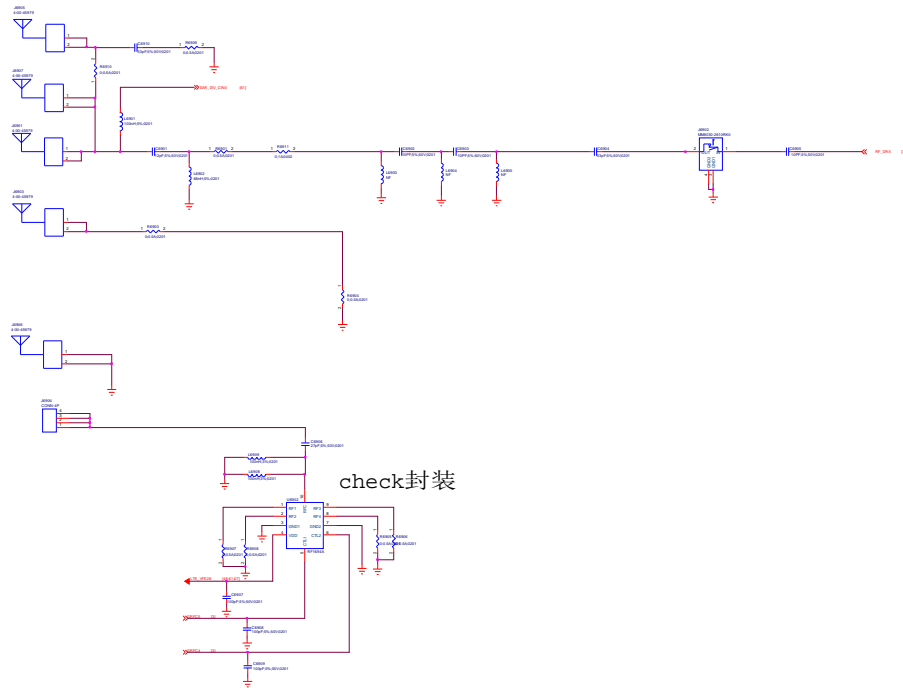
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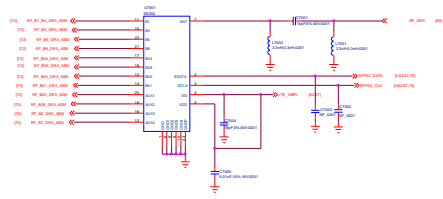
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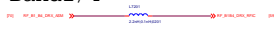


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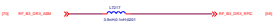
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Author:	Engineering - Mechanical / P. J. Jones	Checked:	
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AeroSpace Technology, Inc. 10000 10th St. Suite 1000			

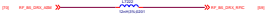
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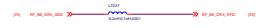
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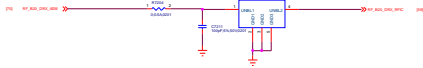
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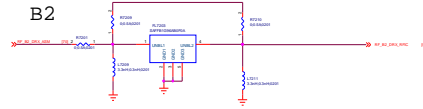
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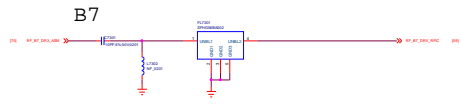


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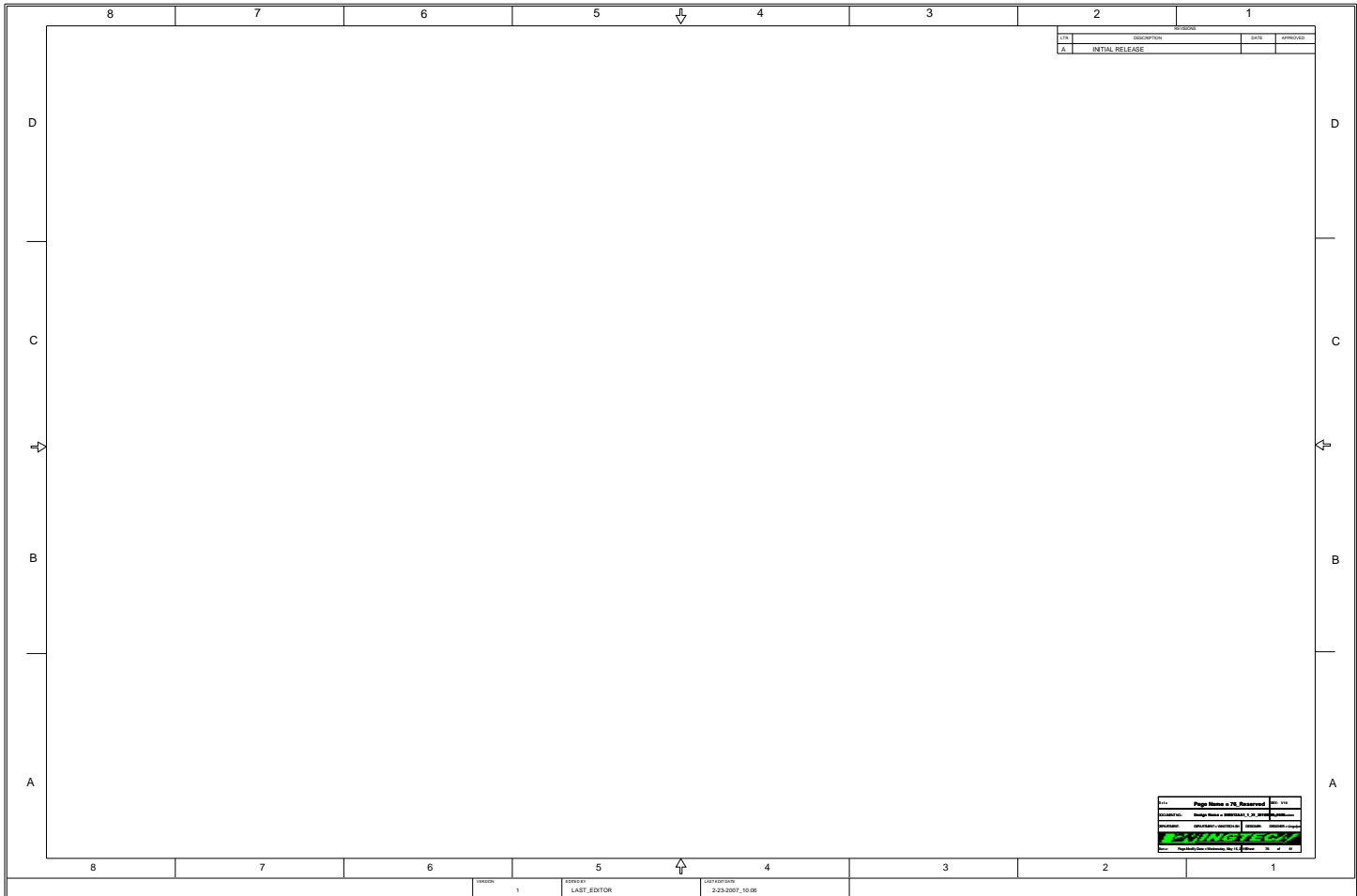
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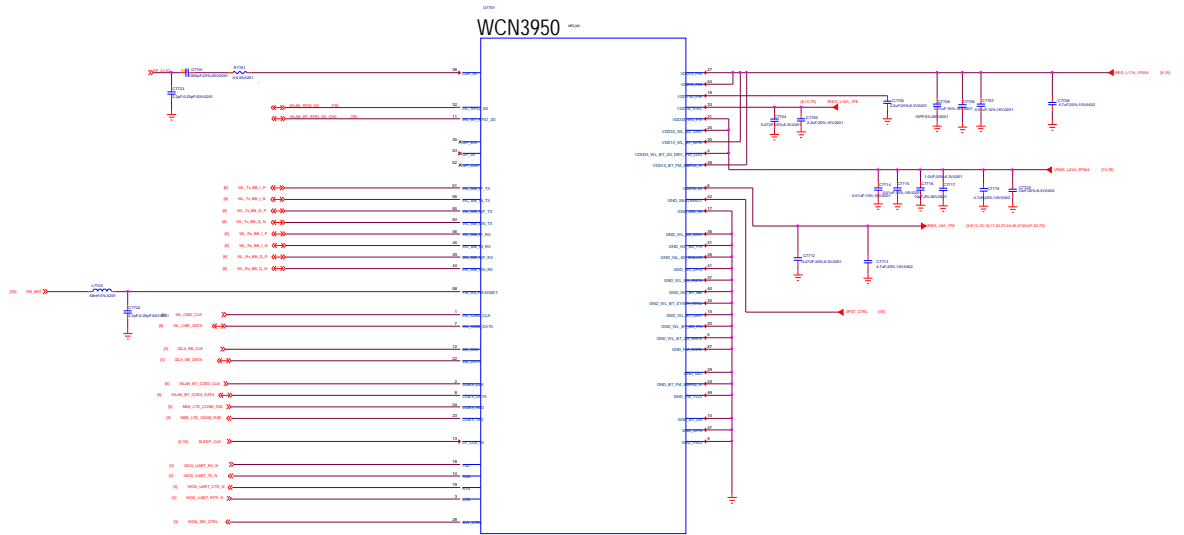


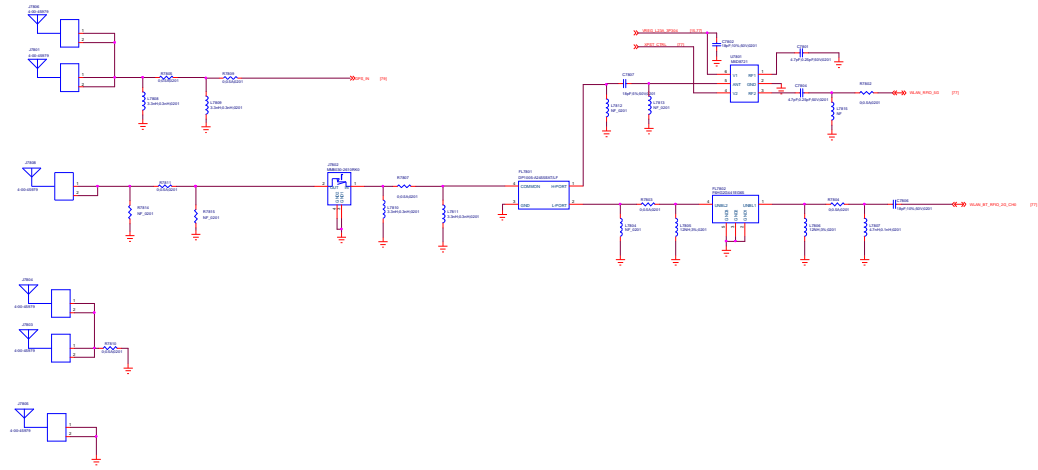


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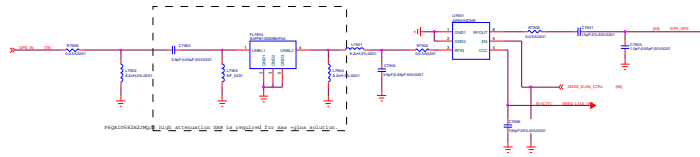


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Description: [Description]		Version: 1.0
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